

A NOVEL COMPUTERIZED MULTIHARMONIC ACTIVE LOAD-PULL SYSTEM FOR THE OPTIMIZATION OF HIGH EFFICIENCY OPERATING CLASSES IN POWER TRANSISTORS.

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ABSTRACT

A fully automated multiharmonic load-pull system allowing accurate measurement and control of the first three harmonic load terminations of RF and microwave transistors is presented in this paper.

The technical originality of the proposed system lies in that the first, second and third harmonic load terminations can be independently and automatically monitored and fixed while varying the input power driving the transistor at the fundamental frequency.

Appropriate hardware and software allow fast and automatic plots of power / efficiency performances of DUTs versus input power for different harmonic loadings.

To demonstrate an attractive application of the system, measurements of a 1800 μm gate periphery MESFET at 1.8 GHz for mobile communication applications are presented.

Both suitable harmonic load terminations and non-appropriate ones yielding respectively optimum and poor power added efficiency are given.

INTRODUCTION

The design of high efficiency power amplifiers is one of the major challenge in the field of mobile radio-systems and active phased-array radars.

During the past few years, a great effort has been performed in the research and elaboration of new and promising semiconductor devices. Impressive progress in fabrication of heterojunction bipolar transistors (HBT) and wide bandgap semiconductor MESFETs (SiC and GaN) have been accomplished.

The need of accurate and sophisticated measurement systems to determine the performances and limitations of such devices for high efficiency power amplification has become crucial.

Measurement setups using the active load-pull approach are now widely adopted. [1], [2], [3]. However, conventional load-pull systems suffer in that they don't allow the measurement and control of harmonics.

It is well known that significant improvements in power transistor efficiency are achieved by properly tuning harmonics.

Therefore, multiharmonic load-pull systems reveal to be the most suitable measurement tools to determine the best achievable power added efficiency and associated operating conditions of transistors : (bias voltages and currents, power level and harmonic load terminations).

Few systems allowing measurements of fundamental and higher harmonics have been proposed [4], [5].

[4] propose a setup in which a microwave transition analyzer is used as fundamental and harmonic receiver.

[5] propose a setup including a vector network analyzer locked at harmonics frequencies while driving the device under test at the fundamental frequency.

Nevertheless, these systems don't allow the control of harmonic loadings in order to obtain time waveforms required to maximize power / efficiency performances of transistors.

Active load-pull systems including second harmonic injection ($2f_o$) at the output of the device under test have been proposed [6], [7]. There are two main difficulties encountered when using such setups.

- First at all, as far as second harmonic injection affects significantly fundamental frequency performances (which is in fact the wanted phenomena to improve efficiency in amplifiers), the fundamental load impedance is not kept constant while varying injection conditions at $2f_o$. Therefore, the load-impedance at f_o may pull away from its optimum value.

If the transistor is tuned again, the second harmonic load termination varies and may yield poor power added efficiency.

- Moreover, load impedances at (f_o and $2f_o$) don't remain constant while varying the input power driving the transistor under test since load-impedances at different harmonics are interdependent and are strongly dependent on the input power level of the device under test.

This implies that a great number of difficult and time-consuming measurements is necessary to reach optimum operating conditions. This major difficulty will be greatly increased if the control of the three first harmonics is envisaged.

To overcome these drawbacks, a novel multiharmonic load-pull technique providing an attractive solution is described in this paper.

It is based on the use of three active loops running respectively at f_o , $2f_o$ and $3f_o$ to synthesize harmonic load terminations.

I - PRINCIPLE OF THE LOAD-PULL TECHNIQUE BY USING ACTIVE LOOPS

Basically, they are two main techniques to perform active load tuning of transistors.

For the first one, a power source, independent of the transistor under test is used to drive the output port (**figure 1**).

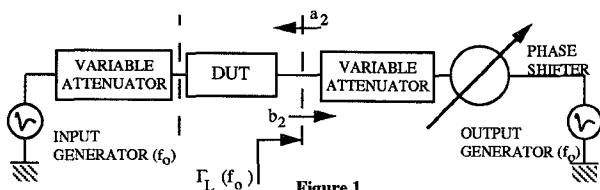


Figure 1

Any load impedance $\Gamma_L(f_o)$ can be synthesized by varying the phase shifter and the attenuator connected to the output of the DUT.

One of the major difficulty encountered when using this technique is that the load-impedance is not kept constant while varying the power level of the input generator.

The second method consists in using an active loop to synthesize load impedances. In that case, the output power wave b_2 delivered by the DUT is coupled, amplified, phase shifted and injected back to the output access of the DUT (**figure 2**) [5].

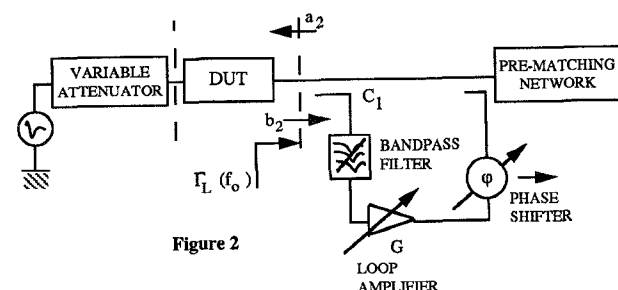


Figure 2

The DUT may be pretuned by adjusting an appropriate passive network (tuner as example) when the loop is turned off. The load impedance Γ_L is controlled by varying the gain and the phase-shift of the loop. A narrow bandpass filter at f_o is necessary to avoid instabilities of the loop. The reflection coefficient of the load impedance is :

$$\Gamma_L = \frac{a_2}{b_2} = \Gamma_o + C_1 \alpha G e^{j\phi}$$

where :

C_1 is the coupling factor, α : the losses of the loop, $G e^{j\phi}$ the complex gain of the loop

and $\Gamma_o = \Gamma_L$ when the loop is turned off.

As far as, the loop gain G remains constant (linear behavior), Γ_L is automatically kept constant while varying the input power driving the DUT. By varying G and ϕ load-impedance loci are generated.

Figures 3a and 3b show the distribution of load-impedances for $\Gamma_o = 0$ (classical method) and for $\Gamma_o \neq 0$ (modified method) [8]. Distribution of points (**figure 3a**) is not always well-suited and may yield poor concentration of measurements in the optimum load-impedance area. A better distribution is achieved (**figure 3b**) if an appropriate adjustment of Γ_o is performed.

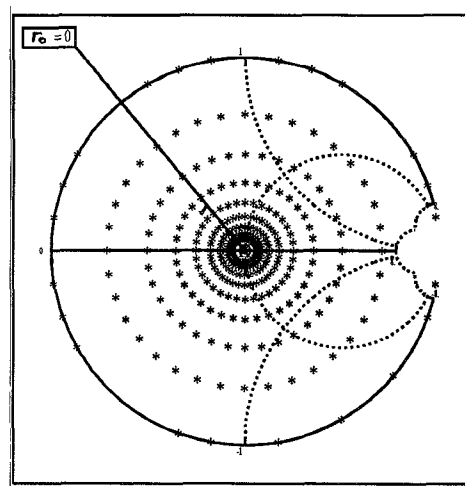


Figure 3a

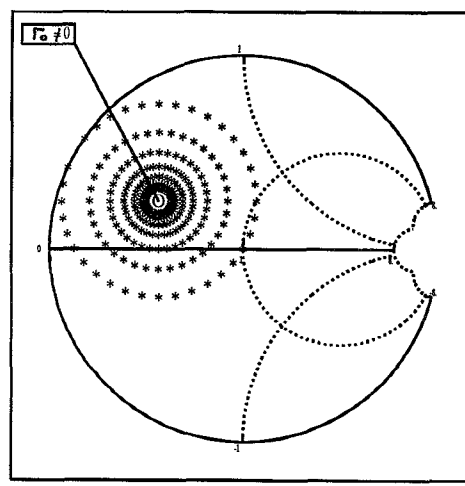


Figure 3b

The block diagram of the load-pull setup we have designed (seeing only at the fundamental frequency operation f_o) is sketched in **figure 4**.

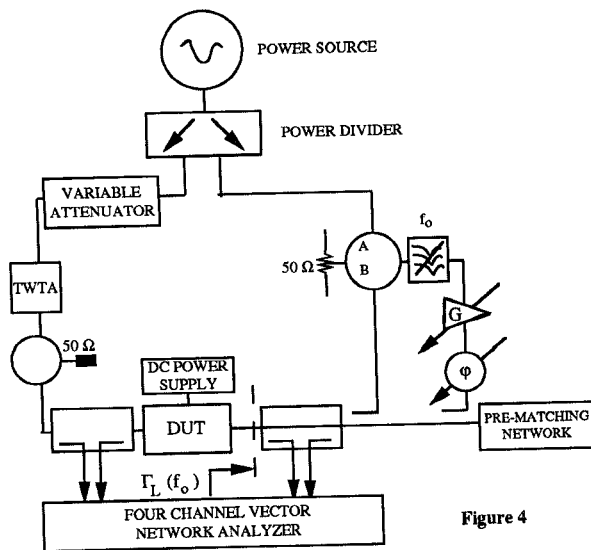


Figure 4

The measurement sequence consists in three main steps.

First, the commutator is switched onto B position and a full two port TRL calibration procedure is performed by using internal capabilities of the vector network analyzer.

-Secondly, the passive pre-matching circuit is tuned so as the DUT is optimally loaded at low power level.

In a third step, the active load-pull procedure is performed so as to determine optimum operating conditions in large signal operation mode.

II - IMPLEMENTATION OF THE TECHNIQUE AT HIGHER HARMONICS

Theoretical analysis have shown that significant improvements in power added efficiency of transistors occur when harmonics are terminated into high-reflective load impedances (short circuit-open circuit). From an experimental point of view, a multiharmonic setup must allow the synthesis of large reflection coefficients (close to the edge of the Smith Chart) at $2f_0$, $3f_0$ while maintaining the load impedance off f_0 in a confined area where the best power amplification capabilities of the transistor are reached.

The above requirements are met within the appropriate hardware of the multiharmonic load-pull system sketched in figure 5.

In the measurement setup of figure 5, a four channel vector network analyzer (VNA) is used in a receiver operation mode allowing so measurements of power wave ratios at harmonics ($2f_0$ - $3f_0$) while driving the device at the fundamental frequency f_0 .

No special filtering is needed in the measurement channels because the VNA is used as a frequency selective wave meter.

Methodology of measurement

- First at all commutators K_1 , K_2 , K_3 are alternately switched onto B position. A full two port calibration procedure is performed at the fundamental frequency f_0 . A one port calibration sequence is achieved at $2f_0$ and $3f_0$. A full two

port calibration procedure should be completed at $2f_0$ and $3f_0$ but it is not required for our application.

In a second step, the attenuator α_0 and the phase shifter ϕ_0 are adjusted so as to pretune the DUT at f_0 . This task is achieved when the three active loops are tuned off.

As a starting condition for the load-pull process, α_0 and ϕ_0 may be tuned so as the DUT is optimally loaded for low level operation.

- In a third step, the loop at the fundamental frequency f_0 is turned on and the load impedance yielding maximum power added efficiency is researched.

- In a fourth step, the loop at the second harmonic frequency ($2f_0$) is turned on and the load impedance at $2f_0$ providing the largest increase of the power added efficiency is researched and fixed.

The key point of our system is that the load-pull process at $2f_0$ doesn't modify the load-impedance at f_0 which has been previously synthesized by the first loop.

- In a fifth step, similar operations are performed at the third harmonic without affecting load impedances at f_0 and $2f_0$.

Finally, the three harmonic load terminations are fixed at their optimum values and a power sweep at f_0 at the input of the DUT is achieved to obtain optimum power efficiency characteristics.

A 1800 μm gate periphery 0,7 μm gate length MESFET (Thomson HP 07) has been measured.

Figures 6 and 7 show the effect of second harmonic loading on added power and power added efficiency (the third harmonic is terminated into a 50 Ω load).

Curves highlight the significant influence of harmonic loadings on performances of power transistors.

Figure 8 shows the influence of the third harmonic loading on power added efficiency in the case of an optimally loaded DUT at f_0 and $2f_0$.

CONCLUSION

The proposed multiharmonic load-pull system allows an experimental simulation of high efficiency operating classes in power transistors at microwave frequencies.

One of its main use is in the optimization of power amplifiers for mobile communication systems and phased-array radars. Furthermore, this characterization tool is expected to be very useful for the validation of nonlinear modeling techniques. Further investigations on gain compression or expansion mechanism can be also carried-out.

REFERENCES

- [1] J.M. NEBUS and al. "Optimized CAD of power amplifiers for maximum added power or minimum third order intermodulation using an optimization software coupled to a single tone source and load-pull setup". *IEEE MTT - Int. Microwave Symposium Digest*, pp 1049-1052, 1988.
- [2] K. KOTZEBUE and al. "An 18 to 26.5 GHz waveguide load-pull system using active load-tuning". *IEEE MTT - Int. Microwave Symposium Digest*, pp 455-456, 1987.
- [3] D.A. TEETER and al. "Large signal characterization and numerical modeling of the GaAs / AlGaAs HBT". *IEEE MTT - Int. Microwave Symposium Digest*, pp 651-654, 1991.
- [4] F.V. RAAY, G. KOMPA "A new on-wafer large signal waveform measurement system with 40 GHz harmonic bandwidth". *IEEE MTT - Int. Microwave Symposium Digest*, pp 1435-1438, 1992.
- [5] B. HUGHES and al. "Accurate on-wafer power and harmonic measurements of microwave amplifiers and devices". *IEEE MTT - Int. Microwave Symposium Digest*, pp 1019-1022, 1992.
- [6] Y. IKEDA and al. "High efficiency operation of FET using second harmonic injection method". *The 3rd Asia Pacific Microwave Conference Proceedings*, pp 685-688, 1990.
- [7] P. BERINI and al. "An experimental study of the effects of harmonic loading on microwave MESFET oscillators and amplifiers". *IEEE Transactions on Microwave Theory and Techniques*, Vol. 42, pp 943-950, 1994.
- [8] Ph. BOUYSSSE and al. "A novel accurate load-pull setup allowing the characterization of highly mismatched power transistors". *IEEE Transactions on Microwave Theory and Techniques*, Vol. 42, pp 327-332, February 1994.

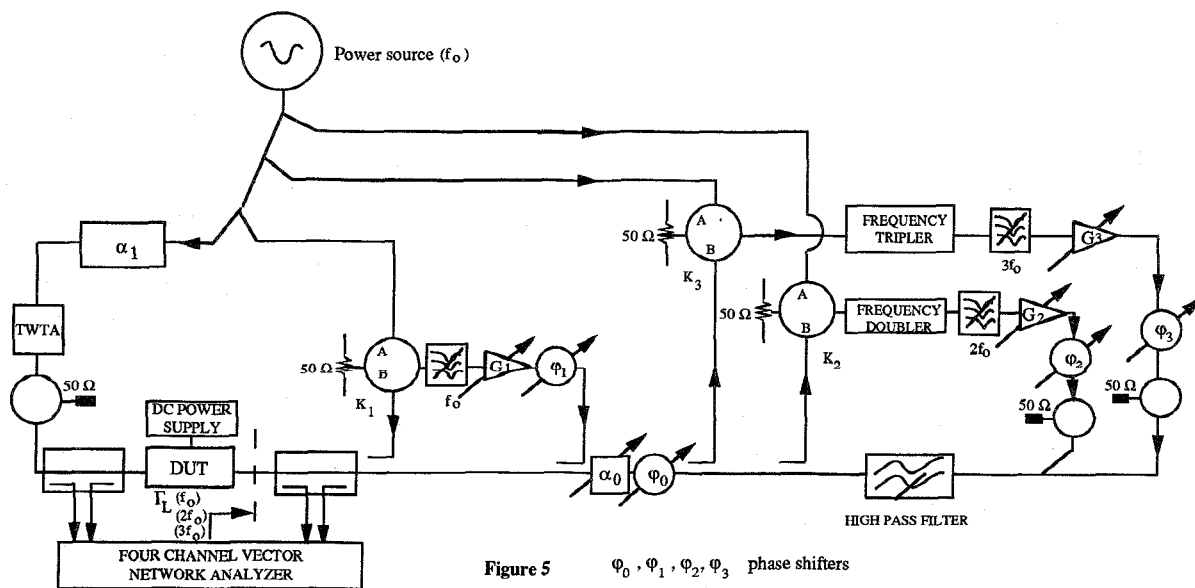
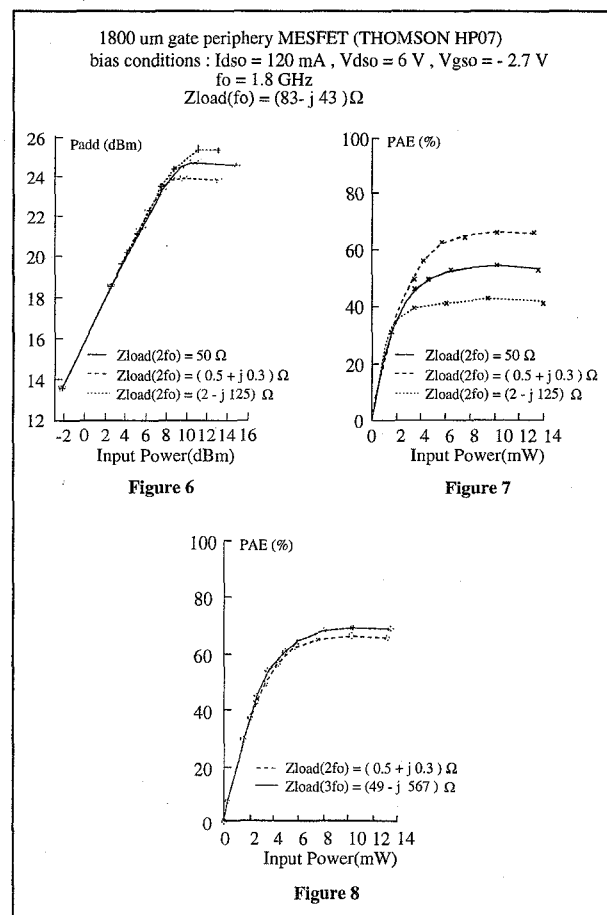


Figure 5